CLAIMS:

1. A coarse delay tuner circuit for use with delay locked loops, said coarse delay tuner circuit comprising:
an input node for receiving an input signal, wherein said input signal is a clock signal;
a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit is adapted to condition said input signal and to provide a first output signal in response to a threshold level being reached by said input signal;
an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit is adapted to receive said first output signal, said edge suppressor circuit adapted to provide a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal; and
an output node for outputting said third output signal.

2. The coarse delay tuner circuit of claim 1, further comprising a signal conditioning circuit operationally connected to said input node, said signal conditioning circuit adapted to prepare said input signal for use by said triggering circuit.

3. The coarse delay tuner circuit of claim 2, wherein said signal conditioning circuit is a low pass filter circuit.

4. The coarse delay tuner circuit of claim 3, wherein said low pass filter circuit is a first order R-C network.

5. The coarse delay tuner circuit of claim 1, wherein said triggering circuit is a Schmitt trigger circuit.

6. The coarse delay tuner circuit of claim 1, wherein said edge suppressor circuit further comprises:

a first D-flipflop, said first D-flipflop having a clock input connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate;

an inverter connected to said first output signal for producing an inverted input signal;

a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flipflop;

said first NAND gate having an output connected to a second input of a second NAND gate; and

said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for providing said third output signal.

7. The coarse delay tuner circuit of claim 1, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period relative to the clock signal.

8. A method for reducing lock time in a delay locked loop (DLL), said method comprising:

providing an input node for receiving an input signal, wherein said input signal is a clock signal;

providing a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit is adapted to condition said input signal and to provide a first output signal in response to a threshold level being reached by said input signal;

providing an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit is adapted to receive said first output signal, said edge suppressor circuit adapted to provide a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal; and

providing an output node for outputting said third output signal.

9. The method of claim 8, further comprising a signal conditioning circuit operationally connected to said input node, said signal conditioning circuit adapted to prepare said input signal for use by said triggering circuit.

10. The method of claim 9, wherein said signal conditioning circuit is a low pass filter circuit.

11. The method of claim 10, wherein said low pass filter circuit is a first order R-C network.

12. The method of claim 8, wherein said triggering circuit is a Schmitt trigger circuit.

13. The method of claim 8, wherein said edge suppressor circuit further comprises:

a first D-flipflop, said first D-flipflop having a clock input connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate;

an inverter connected to said first output signal for producing an inverted input signal;

a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flipflop;

said first NAND gate having an output connected to a second input of a second NAND gate; and

said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for outputting said third output signal.

14. The method of claim 8, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period relative to the clock signal.

15. A semiconductor device with a synchronous memory component, said semiconductor device comprising:
a reference clock signal applied to said synchronous memory component; and
a coarse delay tuner circuit for reducing lock time in said synchronous memory component.

16. The semiconductor device of claim 15, wherein said coarse delay tuner circuit further comprises:

an input node for receiving said reference clock signal;

a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit is adapted to condition said reference clock signal and to provide a first output signal in response to a threshold level being reached by said reference clock signal;

an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit is adapted to receive said first output signal, said edge suppressor circuit adapted to provide a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal; and

an output node for outputting said third output signal to said synchronous memory component.

17. The semiconductor device of claim 16, further comprising a signal conditioning circuit operationally connected to said input node.

18. The semiconductor device of claim 17, wherein said signal conditioning circuit is a low pass filter circuit.

19. The semiconductor device of claim 18, wherein said low pass filter circuit is a first order R-C network.

20. The semiconductor device of claim 16, wherein said triggering circuit is a Schmitt trigger circuit.

21. The semiconductor device of claim 16, wherein said edge suppressor circuit comprises:

a first D-flipflop, said first D-flipflop having a clock input connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate;

an inverter connected to said first output signal for producing an inverted input signal;

a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flipflop;

said first NAND gate having an output connected to a second input of a second NAND gate; and

said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for outputting said third output signal.

22. The semiconductor device of claim 16, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period.

23. A method of providing synchronization in a semiconductor device having a synchronous memory component, said method comprising:
providing a reference clock signal applied to said synchronous memory component; and providing a coarse delay tuner circuit for reducing lock time in said synchronous memory component.

24. The method of claim 23, wherein said coarse delay tuner circuit further comprises:

an input node for receiving said reference clock signal;

a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit is adapted to condition said reference clock signal and to provide a first output signal in response to a threshold level being reached by said reference clock signal;

an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit is adapted to receive said first output signal, said edge suppressor circuit adapted to provide a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal;

an output node for outputting said third output signal to said synchronous memory component.

25. The method of claim 24, further comprising a signal conditioning circuit operationally connected to said input node.

26. The method of claim 25, wherein said signal conditioning circuit is a low pass filter circuit.

27. The method of claim 26, wherein said low pass filter circuit is a first order R-C network.

28. The method of claim 24, wherein said triggering circuit is a Schmitt trigger circuit.

29. The method of claim 24, wherein said edge suppressor circuit comprises:

a first D-flipflop, said first D-flipflop having a clock input connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate;

an inverter connected to said first output signal for producing an inverted input signal;

a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flipflop;

said first NAND gate having an output connected to a second input of a second NAND gate; and

said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for outputting said third output signal.

30. The method of claim 24, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period.

31. An apparatus containing a synchronous integrated circuit, said apparatus comprising:

a synchronous memory component;

a reference clock signal applied to said synchronous memory component; and

a delay locked loop, wherein said delay locked loop includes edge suppressor means for reducing lock time in said synchronous memory component.